**20 Simple Goal-Oriented Queries**

Show the overall yield performance of the latest lot.

List weekly wafer-level yield values.

Display a summary of passing vs. failing dies on the most recent wafer.

Monitor yield performance for the past month.

Provide a table of lot-level yields for the current quarter.

Report the number of failing dies on the last tested wafer.

Show test bin counts for the latest lot.

List test measurements that resulted in failing outcomes for a selected wafer.

Highlight any wafers with yield below the target of 95%.

Provide a summary of logical test outcomes for the current week.

Display the average parametric test value for a chosen test measurement.

Generate a simple yield trend chart for the past three weeks.

List the top three test bins with the highest failure counts.

Summarize the number of E-test measurements per wafer.

Show the pass/fail status of each test program for a specific wafer.

Provide a breakdown of yield performance by test house for the latest lot.

Report the number of dies tested on the last wafer.

Display the weekly count of wafers with an edge-ring failure pattern.

List the average yield for wafers in the most recent lot.

Generate a report on the total number of tests executed last week.

**20 Moderate Goal-Oriented Queries**

Identify trends in wafer-level yield over the last quarter.

Compare yield performance between two consecutive lots.

List wafers with a consistent yield below 95% over multiple weeks.

Analyze the distribution of failing dies across different test bins.

Identify which test measurements most frequently lead to failing dies.

Correlate the frequency of a specific test bin failure with lot yield.

Track yield performance per tester across multiple weeks.

Report the variability of parametric test values for a specific measurement.

Compare logical test failure rates across different test programs.

Summarize yield performance differences between multiple test houses.

Identify the top three test programs contributing to yield drop.

Analyze wafer map patterns for lots with anomalous yield.

Compare E-test measurement variations between high-yield and low-yield wafers.

Identify if yield performance is trending down over the last 10 lots.

Compare the yield impact of different probe configurations (e.g., 12x12 vs. others).

Analyze the distribution of failures across different regions of a wafer.

Track changes in test measurement performance across a specified time period.

Identify clusters of failing dies on wafers with below-target yield.

Analyze the effect of tester variation on yield performance.

Compare yield performance for wafers tested under different load board configurations.

**20 Complex Goal-Oriented Queries**

Determine the correlation between yield drops and specific manufacturing process changes.

Identify the primary test measurement(s) causing yield issues across multiple lots.

Correlate unusual wafer map patterns (e.g., clusters or grid patterns) with specific test programs.

Analyze the impact of a change in probe configuration on the overall lot yield.

Correlate trends in E-test measurements with fluctuations in lot-level yield.

Identify if a particular test house is consistently associated with lower yields.

Analyze yield performance by correlating logical and parametric test failures.

Identify the key test bins driving yield issues and their associated failure modes.

Correlate die failure clusters with manufacturing process adjustments across consecutive lots.

Determine if an increase in parametric test variance correlates with a yield drop.

Analyze the impact of tester-specific load board configurations on yield performance.

Identify correlations between test measurement statistics and E-test fluctuations.

Compare yield performance before and after adjustments to the test process.

Determine if specific failure patterns (e.g., edge-ring vs. center) relate to manufacturing anomalies.

Correlate yield drops with specific changes in foundry settings over a period of three months.

Analyze whether changes in a family of voltage measurements correlate with lot-level yield trends.

Determine if yield issues can be traced to specific subgroups of test measurements across wafers.

Identify the impact of tester-to-tester variability on overall yield performance.

Analyze the statistical significance of test bin failures on predicting yield drops.

Correlate the spatial distribution of failing dies with specific manufacturing process adjustments and suggest possible corrective actions.

**Multi Goal-Oriented Queries**

For the most recent 10 lots from test house A, identify lots with yield below 95%, determine which test bins contribute most to the failing dies, and investigate whether the same bins are also dominant in other test houses.

Track the weekly wafer-level yield trend for product XYZ, flag weeks with sharp yield drops, and correlate those weeks with changes in E-test site statistics or equipment used.

Detect any recurring wafer map patterns (e.g., edge-ring or grid) in wafers with <90% yield over the past quarter, and assess whether these patterns are more common in certain probe card IDs or test programs.

For all lots tested on tester T001, identify if yield performance changes when the handler or load board changes, and summarize failure modes (bins) that dominate when yield drops.

Compare the soft bin distribution for two consecutive test program revisions of device D123, and determine whether yield change is driven by increased failures in a specific measurement family.

Find all wafers in which the failing dies are concentrated in a particular region (e.g., upper-left or center), analyze if these patterns persist across lots, and identify associated failing test measurements.

Analyze if low-yield wafers from fab F21 show a strong correlation between E-test parameter drift and high failure rate in voltage-related parametric tests, and suggest which wafers may benefit from a process shift.

For lots with <93% yield tested at test house B over the past month, evaluate if retesting the worst wafer improves lot yield significantly, and determine what test bins are reduced through retest.

Cluster the wafers by their soft bin profile over the last 100 lots and identify clusters that consistently fall below target yield; investigate if any of these clusters are linked to specific PCM outliers.

Detect whether any changes in prober or load board usage over time coincide with increased failing dies in logical test measurements, especially for test bins 10-20.

Monitor the yield of project X456 over the last 6 months, flag lots below target yield, identify the test bin(s) and test program(s) most responsible, and determine if failure rates increase at specific test sites.

Compare the E-test parameter distributions of high-yield vs low-yield lots in product line ABC123, and identify if any site-level E-test metrics show statistically significant separation between the two groups.

Find whether the same test measurements that caused failures in the top 5 low-yield wafers this month also appeared in other wafers with normal yield; analyze if these failures were masked by bin limits.

Detect if yield loss is consistently higher when the probe touches the wafer at specific locations, suggesting mechanical misalignment, and correlate these touches with wafer map patterns.

Examine if consecutive lots with voltage-related test failures are tested on the same equipment chain (test house → tester → load board), and suggest if a hardware issue may be involved.

For the latest 50 lots, evaluate if failures in bin 25 correlate with environmental temperature changes during testing, and compare this bin’s rate across different test houses.

Determine if project DEF789’s low yield is due to a shift in E-test metrics at the wafer edge; correlate edge site E-test values to failing die locations and recommend whether a process change is needed.

Identify test measurements with high variance across wafers and analyze whether this variance explains the difference in yield between wafers in the same lot.

Monitor for repeating wafer map checkerboard patterns in failing dies and evaluate whether these patterns correlate with test program configurations or equipment calibration intervals.

Compare the yield recovery after re-probing for lots with known voltage test failures, and assess whether test bin classification changed significantly between first and second probe attempts.